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IMPORTANT INFORMATION: PLEASE READ BEFORE USING HSC600 / HSC601.



High Speed Counter (HSC) Self-Help Guide

This guide covers:

HE*800*HSC600/601 and HE*820*HSC600/601 **SmartStack** modules. HE500OCS033/063 and HE500OCS034/064 **MiniOCS** modules HE500RCS063 and HE500RCS064 **MiniRCS** modules. This guide also covers HSC products starting with IC300.

NOTE: Examples in this guide refer to SmartStack modules, but information applies to other products listed above.

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What High Speed Counter Option do I choose?

Note: The Selection Guide below refers to chapters found in the HSC Supplement (SUP0265). See **Technical Support** at the end of this document to locate and download the supplement from the web.

High Speed Counter Option Selection Guide



* Option 7 is Similar to Option 2 except edge triggered enable and one shot on clear. See Chapter 4 in the HSC Supplement (SUP0265) for details.

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NOTES

Which OCS Registers are used with the High Speed Counter?

High Speed Counter Cscape I/O Summary

Note: The summary below refers to chapters found in the HSC Supplement (SUP0265). See *Technical Support* at the end of this document to locate and download the supplement from the web.

%I Data Registers

Note: A key is attached to this table that explains conventions used in the HSC register tables.

Register		Option 1	Option 2/7	Option 3	Option 4
%l1	11 /	CLK 1	I1 / CLK 1	I1 / Encoder A	I1 / Encoder A1
%l2	12 /	DIR 1	l2 / DIR 1	I2 / Encoder B	I2 / Encoder B1
%I3	13 /	CNTRL 1	I3 / CNTRL 1	13 / Encoder M	I3 / Encoder M1
%14	I4 /	CNTRL 1	I4 / CNTRL 1	I4 / Enc. M Disable	I4 / Enc. M1 Disable
%I5	15 /	CLK 2	15 / CLK 2	15	I5 / Encoder A2
%16	l6 /	DIR 2	16 / DIR 2	16	I6 / Encoder B2
%17	17 /	CNTRL 2	17 / CNTRL 2	17	I7 / Encoder M2
%18	18 /	CNTRL 2	18 / CNTRL 2	18	18 / Enc. M2 Disable
%19	Gat	e for Freq.		%Q1 Image	
%l10	PW	M 1		%Q2 Image	
% 11	PW	M 2		%Q3 Image	
%l12	Res	served	Not Applicable to	%Q4 Image	Not Applicable to
%l13	Res	served	Option.	%Q5 Image	Option.
% 14	Res	served		%Q6 Image	
%l15	Res	served		%Q7 Image	
%l16	Res	served		%Q8 Image	
			Key For Regis	ster Tables	
Registers are set to 0.					
Not Applicabl	e to	These tables ser	ve as a general reference for	or the starting location of the re	egisters. To determine the
Option.		Cscape Software	e after configuration.	ers, it is necessary to consult i	the I/O map screen in the
%l1-8		User Inputs if not	t assigned to another function	on.	
CLK 1 / 2		Refers to Clock '	1 / Clock 2. The Counter c	ounts on each positive Clock	edge.
		Refers to Direction	on 1 / Direction 2 The Clo	ck Direction input (if used) ca	uses an up count (when the
		input is a logic hi	igh) and a down count (whe	en the input is a logic low).	abes an up bount (when the
				,	
		Note: The Quad	arature Mode of Option 1, 2	, and / counters operates much be Clock and Direction input	the same as the
		Channel A and C	Channel B. The normal Cloc	k input becomes Channel A, a	and the normal Direction
		input becomes C	Channel B. The phase relation	onship of Channel A and Char	nel B determines the count
		direction.	1/Control 2 Cas Times	of Control Cignolo in this mid-	(none Fureni Deelymenk sof
GNIKL 1/2		defined.).	1 1/ Control 2. See Types C	or Control Signals in this guide	(page Error! Bookmark not

%AI Data

Note:	A key	is attached	to this	table that	explains	conventions	used in	the HSC	register	tables.

Register	Option 1	Option 2 / 7	Option 3	Option 4
%Al1	Option Number	Option Number	Option Number	Option Number
%Al2	Cntr. 1 Value or	Cntr. 1 Value LW	Cntr. 1 Value LW	Cntr. 1 Value
	Freq. LW			
%AI3	Cntr. 1 Value or	Cntr. 1 Value HW	Cntr. 1 Value HW	Cntr. 2 Value
	Freq. HW			
%Al4	Cntr. 2 Value or	Cntr. 2 Value LW		
	Freq. LW			
%AI5	Cntr. 2 Value or	Cntr. 2 Value HW		
	Freq. HW			
%Al6	Cntr. 1 Latch	Cntr. 1 Latch		
	Value LW	Value LW	Not Applicable to	Not Applicable to
%AI7	Cntr. 1 Latch	Cntr. 1 Latch	Option.	Option.
	Value HW	Value HW		
%Al8	Cntr. 2 Latch	Cntr. 2 Latch		
	Value LW	Value LW		
%AI9	Cntr. 2 Latch	Cntr. 2 Latch		
	Value HW	Value HW		
		Key For Register	Tables	
Not Applicable t	 These tables serve a 	as a general reference for th	e starting location of the reg	jisters. To determine the
Option.	actual starting locati	on of the various registers,	it is necessary to consult th	e I/O Map screen in the
IW		er conliguration.		
	High Word of DINT			
CNTR 1/2	Refers to Counter 1	Counter 2		

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%Q Data

Note: A key is attached to this table that explains conventions used in the HSC register tables.

Register	Option 1	Option 2/7	Option 3	Option 4
%Q1	Q1 / PWM 1	Q1 / Cntr. 1 SP 1	Q1 / CAM 1	Q1 / CAM 1-1
%Q2	Q2	Q2 / Cntr. 1 SP 2	Q2 / CAM 2	Q2 / CAM 2-1
%Q3	Q3	Q3	Q3 / CAM 3	Q3 / CAM 3-1
%Q4	Q4	Q4	Q4 / CAM 4	Q4 / CAM 4-1
%Q5	Q5 / PWM 2	Q5 / Cntr. 2 SP 1	Q5 / CAM 5	Q5 / CAM 1-2
%Q6	Q6	Q6 / Cntr. 2 SP 2	Q6 / CAM 6	Q6 / CAM 2-2
%Q7	Q7	Q7	Q7 / CAM 7	Q7 / CAM 3-2
%Q8	Q8	Q8	AF / CAM 8	AF / CAM 4-2
%Q9	AF	AF	AF	AF
%Q10	AF	AF	AF	AF
%Q11	AF	AF	AF	AF
%Q12	AF	AF	AF	AF
%Q13	AF	AF	AF	AF
%Q14	AF	AF	AF	AF
%Q15	AF	AF	AF	AF
%Q16	AF	AF	Reserved	Reserved
%Q17	AF	Reserved	AF	AF
%Q18	AF	Reserved	AF	AF
%Q19	AF	AF	AF	AF
%Q20	Reserved	AF	Reset	Reset 1
%Q21	Reserved	AF	Reserved	AF
%Q22	Reserved	AF	Reserved	AF
%Q23	Reserved	Reserved	Reserved	AF
%Q24	Reserved	Reserved	Reserved	Reset 2
%Q25	Load 1	Load 1	AF	AF
%Q26	Enable 1	Enable 1	AF	AF
%Q27	Clear 1	Clear 1	AF	AF
%Q28	Latch 1	Latch 1	AF	AF
%Q29	Load 2	Load 2	AF	AF
%Q30	Enable 2	Enable 2	AF	AF
%Q31	Clear 2	Clear 2	AF	AF
%Q32	Latch 2	Latch 2	AF	AF
This table is conti	nued on next page.			
		Key For Register Ta	ables	
Reserved	Registers are set to 0.	• • • • • • • • • • • • • • • • • • •		
AF	See manual - refers to A	dvanced Functions cover	ed in the HSC Suppleme	ent (SUP0265).
%Q1-8	User Outputs if not assig	gned to another function.		
CNTR 1 / 2	Refers to Counter 1 / Co	ounter 2.		
SP1 / 2	Refers to Setpoint 1 / Set	etpoint 2.		

%Q Data continue	ed			
Register	Option 1	Option 2/7	Option 3	Option 4
%Q33	AF	AF	AF	AF
%Q34	AF	AF	AF	AF
%Q35	AF	AF	AF	AF
%Q36	AF	AF	AF	AF
%Q37	AF	AF	AF	AF
%Q38	AF	AF	AF	AF
%Q39	AF	AF	Reserved	AF
%Q40	AF	AF	Reserved	AF
%Q41	Pulse 1 Trigger	AF		
%Q42	AF	AF		
%Q43	AF	AF		
%Q44	AF	AF		
%Q45	Pulse 2 Trigger	Reserved		
%Q46	AF	Reserved		
%Q47	AF	Reserved		
%Q48	AF	Reserved	Not Applicable	Not Applicable to
%Q49	AF	to Option.	Option.	
%Q50	AF			
%Q51	AF			
%Q52	AF	Not Applicable to		
%Q53	Reserved	Option.		
%Q54	Reserved			
%Q55	Reserved			
%Q56	Reserved			
		Key For Register Ta	ables	
Reserved	Registers are set to 0.			
AF	See manual - refers to	Advanced Functions cover	ed in the HSC Suppleme	nt (SUP0265).
Not Applicable to Option.	These tables serve as a actual starting location Cscape Software after	a general reference for the st of the various registers, it is configuration.	arting location of the regine necessary to consult the	sters. To determine the e I/O Map screen in the

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%AQ Data

Note: A key is attached to this table that explains conventions used in the HSC register tables.

Register	Option 1	Option 2/7	Option 3	Option 4
%AQ1	Cntr. 1 Load Value or Freq. Time Base LW	Cntr. 1 Load Value LW	Low Set-Point 1 LW	Cntr. 1 Low Set-Point 1
%AQ2	Cntr. 1 Load Value or Freq. Time Base HW	Cntr. 1 Load Value HW	Low Set-Point 1 HW	Cntr. 1 High Set-Point 1
%AQ3	Cntr. 2 Load Value or Freq. Time Base LW	Cntr. 2 Load Value LW	High Set-Point 1 LW	Cntr. 1 Low Set-Point 2
%AQ4	Cntr. 2 Load Value or Freq. Time Base HW	Cntr. 2 Load Value HW	High Set-Point 1 HW	Cntr. 1 High Set-Point 2
%AQ5	Cntr. 1 PWM * Cycle Time **	Cntr. 1 ON Set-Point 1 LW	Low Set-Point 2 LW	Cntr. 1 Low Set-Point 3
%AQ6	Cntr. 1 PWM * Pulse/On Time	Cntr. 1 ON Set-Point 1 HW	Low Set-Point 2 HW	Cntr. 1 High Set-Point 3
%AQ7	Cntr. 2 PWM * Cycle Time **	Cntr. 1 OFF Set-Point 1 LW	High Set-Point 2 LW	Cntr. 1 Low Set-Point 4
%AQ8	Cntr. 2 PWM * Pulse/On Time	Cntr. 1 OFF Set-Point 1 HW	High Set-Point 2 HW	Cntr. 1 High Set-Point 4
%AQ9		Cntr. 1 ON Set-Point 2 LW	Low Set-Point 3 LW	Cntr. 2 Low Set-Point 1
%AQ10		Cntr. 1 ON Set-Point 2 HW	Low Set-Point 3 HW	Cntr. 2 High Set-Point 1
%AQ11	Not Applicable to	Cntr. 1 OFF Set-Point 2 LW	High Set-Point 3 LW	Cntr. 2 Low Set-Point 2
%AQ12	Option.	Cntr. 1 OFF Set-Point 2 HW	High Set-Point 3 HW	Cntr. 2 High Set-Point 2
%AQ13		Cntr. 2 ON Set-Point 1 LW	Low Set-Point 4 LW	Cntr. 2 Low Set-Point 3
%AQ14		Cntr. 2 ON Set-Point 1 HW	Low Set-Point 4 HW	Cntr. 2 High Set-Point 3
This table is	s continued on next page	ge.		·
* PWM Cy ** Special OFF. A va	cle Time and On Time use for 1 and 0: A va lue of 0 sets the cycle	e are in 100ns (0.1us) ir lue of 1 in %AQ5 or %A e time to its maximum v	AQ7 causes the PWN AQ7 causes the PWN value of 6.5535ms.	to 3,2767ms. I output to remain
		Key For Register	Tables	
Not Application to Option.	ble These tables serve as starting location of the Software <i>after</i> configure	a general reference for the star various registers, it is necessa ation.	ting location of the registers. ry to consult the I/O Map so	. To determine the <i>actual</i> creen in the Cscape
LW	Low Word of DINT.			
HW	High Word of DINT.			
CNTR 1 / 2	Refers to Counter 1 / C	Counter 2.		

Register Option 1 Option 2/7 Option 3 Option 4 %AQ15 Cntr. 2 OFF High Set-Point 4 LW Cntr. 2 Low Set-Point 4 LW	1 Point 4
%AQ15 Cntr. 2 OFF High Set-Point 4 LW Cntr. 2 Low Set-Point	Point 4
Set-Point 1 LW	
%AQ16 Cntr. 2 OFF High Set-Point 4 HW Cntr. 2 High Set-Poi	Point 4
Set-Point 1 HW	
%AQ17 Cntr. 2 ON Low Set-Point 5 LW Cntr. 1 Cnts per	
Set-Point 2 LW Revolution	
%AQ18 Cntr. 2 ON Low Set-Point 5 HW Cntr. 2 Cnts per	
Set-Point 2 HW Revolution	
%AQ19 Cntr. 2 OFF High Set-Point 5 LW	
Set-Point 2 LVV	
%AQ20 Cntr. 2 OFF High Set-Point 5 HW	
Set-Point 2 HW	
WAQ21 Not Applicable to Low Set-Point 6 LW	
WAQ22 Option.	
MAQ23 High Set-Point 6 LW	
MAQ24 High Set-Point 6 HW	hla ta
%AQ25 Low Set-Point 7 LW Not Applicable %AQ25 Low Set-Point 7 LW Option	Die to
%AQ20 Low Set-Point / HW Option. 0/ AO27 Not Applicable High Set Doint 7 HW Option.	•
%AQ27 High Set-Point 7 LW	
%AQ28 High Set-Point 7 Hw	
WAQ29	
WAQ30 Low Set-Point 8 HW	
MAQ31 High Set-Point 8 LW	
MAQ32 High Set-Point 8 HW	
%AQ33 Crits per Revolution LVV	
* DVAIA Chuster Time and On Time are in 400mg (0 4ug) in group and form 40ug to 2 0707mg	
[^] PWM Cycle Time and On Time are in 100ns (0.1us) increments from 40us to 3,2767ms.	
** Special use for 1 and 0: A value of 1 in %AQ5 or %AQ7 causes the PWM output to remain	nain
OFF. A value of 0 sets the cycle time to its maximum value of 6.5535ms.	
Key For Register Tables	
Not Applicable These tables serve as a general reference for the starting location of the registers. To determine the actu	actual
to Option. starting location of the various registers, it is necessary to consult the I/O Map screen in the Cscape	;
Software after configuration.	
HW High Word of DINT.	
CNTR 1/2 Refers to Counter 1 / Counter 2	

How do I get started?

High Speed Counter Quick Start Examples

Example 1: Using the Diagnostic Tool (Option 6)

Note: This product has a detailed supplement (SUP0265). See *Technical Support* at the end of this document to locate and download the supplement from the web.

Initial Configuration - Selecting HSC Counter

- 1. For this example, physically install the HSC600 SmartStack module in the *first* I/O slot of the controller. (You can use the HSC601 instead.)
- In Cscape, double-click on the first slot or click on the Config button to its right. A screen appears; click Other tab and then another screen appears. Select HE800HSC600 and click OK. The following screen appears showing the HSC in the first slot. Now click on the Config button to its right.

ERED CSZID-CACHE	OCS Antenna Mar	
	Shelle.	Carity
High Speed Coarter	000000000000000000000000000000000000000	Conto
Evely	ENDLA STRATE	Cowle
Erety	ENDING TO THE PARTY OF THE PART	Cowly
Evety	Community and the second secon	Courg
Auto Costig System		

Figure 1 - Example 1 - HSC is Shown in First Slot

Note: Ensure that the proper controller is selected. If it is <u>not</u> selected, double-click on the controller and select the desired controller from the pull-down menu or press the **Config** button to its right. Press **OK**.

3. The following screen appears.

Type Starting Ending Number of Register Register Recesses NU NONE NONE 0
providence providence providence
NO INONE NONE D
MAI MONE MONE D
NAG NONE NONE D

Figure 2 - Example 1 - Module Configuration Screen

You need to select an HSC option, so click the **Module Setup** tab.

Note: The I/O slot position that is selected affects the *actual* starting location of various registers. It is necessary to consult this **I/O Map** screen in the Cscape Software *after* configuration.

Configuring HSC using Option 6

4. The following screen appears.



Figure 3 - Example 1 - Option 6 Selected

5. Click Option 6. Press Configure button. The following screen appears.

input !	Signal Conditioning	1
nput Filter.	Input Voltage	Cancel
annaise a	• 24 Vota •	-

Figure 4 - Example 1 - Configuring Option 6

In this example, no configuration selections are needed. Simply press **OK**. The screen in Figure 3 appears again; press the **I/O Map** tab at the top of the screen.

Viewing I/O Map

6. The following screen appears.

Module Model HE000 Description: H	15C800 gh Speed Co	ounter-8 in 1	and 8 neg out	
Type %1 %0 %AI %AQ	Dorting Register	Ending Register 16 16 3 [NONE	Number of Registers	
		0K	Cancel	6nm)

Figure 5 - Example 1 - I/O Map for Option 6

The I/O Map shows the *actual* starting location of various registers for the configured HSC600 located in slot 1.

Information subject to change without notice.

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Click **OK** and then download the configuration to the OCS/RCS. No ladder program is needed for this example.

7. What if the HSC module had been placed in slot 2 instead of slot 1? How would it affect the I/O Map and the *actual* starting location of various registers?

Let us assume that there is a mixed digital I/O module in the *first* position and that the HSC is the *second* module on the stack. After configuration, you check the I/O Map for the HSC module (Figure 7).

Module Cor	nfigu	ration			1
[170 Nap] N	lodule	Setup			
Module Modet H Descriptio	E800H r: Hig	ISD500 h Speed D	ounter-8 in	and 8 neg out	
	Туре	Starting Register	Ending Register	Number of Registers	
	81	9	24	16	
	20	9	24	16	
	8AI	11	3	3	
	%A0	NONE	INONE	0	
		1	OK.	Cancel	Apply

Figure 6 - Example 1 - I/O Map for HSC in Second Slot

Notice that the HSC digital I/O starts at register address 9, and the analog inputs start at 1. Any reference to the digital I/O on the High Speed Counter needs to be offset by the starting register address minus one. (e.g. %I1 on the HSC is located at %I9 in the Cscape register map [%I1 + {9-1} = %I9].)

Viewing Data Watch Window (HSC, Option 6)

8. Finally, go to the Data Watch Window and display %Al2 as an integer. You will see the free-running counter clocked by the 10MHz oscillator.

To show some control over the counter, turn on %Q23 (%Q15 + (9-1) = %Q23), which is the mask bit, and then turn on %Q21 (%Q13 + (9-1) = %Q21), which is the Aux1 bit. The counter stops counting (as a direct result of turning Q21 on) and is cleared to 0.

Turn off %Q21 and the counter resumes counting.

Memory	Value	Туре	Nam
%AI0002	-26114	INT	
%Q0023	OFF	BOOL	
%Q0021	OFF	BOOL	_
د]	10		>

Figure 7 - Example 1 - Data Watch Window

Example 2: Using an Event Counter

When configuring an Event Counter, use Option 1 or 2 or 7 depending on your application. In Example 2, Option 1 is used.

Note: The HSC has a detailed supplement (SUP0265). See *Technical Support* at the end of this document to locate and download the supplement from the web.

Selecting Option 1

 Install the HSC SmartStack module and start the initial configuration (page 11) and perform steps 1-3. In this Example 2, it is assumed that the first slot contains a mixed digital module and the HSC is placed in the second I/O slot.

Module Configuration
1/0 Map Module Setup
Choose an option best suited for your Application:
 Option 1: Two 16-bit PWM channels, Two 32-bit Counters
C Option 2: Two 32-bit Counters with latch and setpoints
C Option 3: One 24-bit 8 Cam Encoder
C Option 4: Two 16-bit 4 Cam Encoders
C Option 5: Custom
C Option 6: Diagnostic Tool
Option 7: Similar to Option 2 edge triggered enable and one shot on clear
Configure >>>
OK Cancel Apply

Figure 1 – Example 2 - Option 1 Selected

2. Select Option 1. Then, click the Configure button.

Configuring HSC Using Option 1

- 3. The HSC Configuration screen for Option 1 appears. Click the check boxes for:
 - 1. Enable Counter 1
 - 2. Under Mode, select 10 MHz Osc
 - 3. Latch, Load, Clear and Enable from Ladder

	Counters		
Counter 1	Counter 2		1
Enable	🗂 Enable		
Mode		Mode	
🕤 Count/Dir 👘 Quadratu	ire 🛛 🧖 Counti	/Dir C Quadrature	
C Up/Down C 10 MHz (Dsc C Up/Do	own C 10 MHz Osc	
Latch, Load, Clear & Enable from Ladder	Latch, from L	Load, Clear & Enable adder	
Ext. Input 3: Load	Ext. Input 7		
Ext. Input 4: Latch	Ext. Input 8		
Lies Ext. Input 2 for Direction		ut Jennut & for Direction	
• Up C Down	C Up	C Down	
Frequency Counter (Uses Counter 1 and 2)	C Channel A C	Channel A & B	1
	0	utputs	
Input Signal Conditioning			
Input Signal Conditioning nput Filter:	_ PWM 1	PWM 2	
Input Signal Conditioning nput Filter: 500 KHz	PWM 1	PWM 2	
Input Signal Conditioning nput Filter: 500 KHz 💌	PWM 1 Enable	PWM 2 Enable Cone Shot	ОК

Figure 2 – Example 2 - Option 1 Configuration

You are now looking at your configuration choices on the screen as shown in **Figure 2**. To complete the configuration, press **OK**. You are now looking at the screen in **Figure 1**. Press the **I/O Map** tab at the top of the screen.

Viewing the I/O Map

4. The following screen appears.

Module 4odel: HE80)escription: I)0HSC600 High Speed C	Counter - 8 ir	n and 8 neg out	
Тур	e Starting Register	Ending Register	Number of Reaisters	5
%	9	24	16	
%Q	9	64	56	
%AI		9	9	
%AI	1	8	8	



Look at the I/O Map as shown in Figure 3. In this example, the High Speed Counter is the second module on the stack and there is a mixed digital I/O module in the first position. Therefore the HSC digital I/O starts at register address 9 and the analog I/O starts at 1. Any reference to the digital I/O on the HSC needs to be offset by the starting register address minus one. (e.g. %I1 on the HSC is located at %I9 in the Cscape register map [%I1 + {9-1} = %I9]).

Click **OK** and then download the configuration to the OCS/RCS. No ladder program is needed for this example.

Viewing Data Watch Window (HSC, Option 1)

5. Now go to the Data Watch Window. Select the Controller pull-down menu in Cscape and click Data Watch. Display %AI2 as a DINT (Double Integer). You will see 0 in the counter.

To allow the counter to count, turn on the enable bit located at %Q34, this is the 26^{th} bit in the HSC register map. With the HSC starting at 9 as shown in the I/O Map of Figure 3, turn on %Q34 (%Q26 + (9-1) = %Q34). You will see the free-running counter clocked by the 10MHz oscillator.

Now, turn off $\[\%Q34\]$ ($\[\%Q26\]$ + (9-1) = $\[\%Q34\]$) the Enable bit. The counter stops counting, and you can see the count value in $\[\%Al2/3\]$.

Note: If Option 7 had been selected, the counter continues to count with the Enable bit turned off, because enable is latched. Turning on the Clear bit, the 27th bit in the HSC register map, turns off the Enable and clears the counter to 0.)

To clear the counter to 0, turn on the Clear bit at %Q35 (%Q27 + (9-1) = %Q35).

Memory	Value	Туре
%A10002	0	DINT
%Q0034	OFF	BOOL
%Q0035	OFF	BOOL
<)))

Figure 4 – Example 2 – Data Watch Window

What Additional Information Is Important To Know?

Data Consistency Issue During Counter Accumulator Register Access (Accumulator Register is <u>not</u> Latched)

Applications required to read the counter accumulator registers *during counter operation* need to employ the *latched* values. Latched values are not required for display purposes. (*Types of Control Signals* are discussed later in this section.)

Issue: The accumulator registers of option 1, 2, 3, and 7 counters contain Double Integer values. (That is, they are 24 or 32 bit registers.) If a count occurs coincident with the controller's access to the accumulator register, **erroneous data can result**. This is <u>not</u> an issue for the option 4 accumulator registers, because they are Integer values. (They are 16 bit registers.) The registers in question are as follows (assuming that the module's AI registers begin at AI1):

See %AI Register Table for more details on page 6 in this guide.

Option 1:

 Al2/3 (Counter 1 count or frequency, use Latch and Al6/7)

 Al4/5 (Counter 2 count or frequency, use Latch and Al8/9)

 Option 2:

 Al2/3 (Counter 1 count, use Latch and Al6/7)

 Al4/5 (Counter 2 count, use Latch and Al6/7)

 Al4/5 (Counter 2 count, use Latch and Al8/9)

 Option 3:

 Al2/3 (Count value, no latch available, use CAM Image)

 Option 4:

 Al2 (Counter 1 count, no latch available, read accumulator directly)

 Al3 (Counter 2 count, no latch available, read accumulator directly)

 Option 7:

 Al2/3 (Counter 1 count, use Latch and Al6/7)

 Al2/3 (Counter 1 count, use Latch and Al6/7)

 Al2/3 (Counter 1 count, use Latch and Al6/7)

Types of Control Signals (Options 1, 2, and 7 only)

Note: The following definitions are taken from the HSC Supplement (SUP0265). See **Technical Support** at the end of this document to locate and download the supplement from the web.

Each counter (if enabled) is controlled by the following control signals.

LOAD: Setting the Load signal to Logic 1 forces the count to the Load Value. The Count remains at the Load value until the Load signal is reset to Logic 0. The count then starts from that value and increments or decrements depending on the direction of the count.

ENABLE: Setting the Enable signal to Logic 1 allows the Counter to count. When the Enable signal of an option 1 or 2 counter is set to Logic 0, counting is inhibited. When the Enable signal of an option 7 counter is set to Logic 0, counting continues. Use the Clear signal to stop counting.

CLEAR: Setting the Clear signal to Logic 1 clears the counter to zero, and the count remains at zero until the Clear signal is reset to Logic 0

LATCH: The current counter value is latched into the counter's Latch register on the rising edge of the Latch signal. The counting function is not disturbed by the latch. The register data is not reloaded until the following Latch signal's rising edge appears.

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NOTES

Technical Support

For assistance and manual updates, contact Technical Support at the following locations:

North America: (317) 916-4274 www.heapg.com email: techsppt@heapg.com

Europe: (+) 353-21-4321-266 www.horner-apg.com

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