Unit 1 Centrepoint, Centre Park Rd.,
Cork, Ireland. Phone ++353 (021) 4321266,
Fax ++353 (021) 4321 826

# Horner

## DMX200 Master Module
## User Manual

| Rev | Date | Written by | Revision |
|---|---|---|---|
| 1.0 | 7-Jan-05 | K. Coleman | First Draft |

HORNER IRELAND
Unit 1 Centrepoint, Centre Park Rd.,
Cork, Ireland. Phone ++353 (021) 4321266,
Fax ++353 (021) 4321 826

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# 1.0. Scope

This specification is intended to define the interface between the OCS family of PLC's and the DMX200 Master module.

# 2.0. Introduction

The DMX512 Master protocol is implemented as an asynchronous embedded protocol on an 8-bit uprocessor based Smartstack module. Due to the limited register set of the DMX module the data is sent from the OCS to the module by a series of pages. A page may contain up to one hundred and twenty four channels at a time ( 124 bytes per page). The data is echanged as packed bytes where the low byte is the first channel and the high byte is the next channel, this best suits the OCS data types and allows the greatest data throughput. The pages are controlled by a handshaking method between the OCS and the DMX module to ensure that no data is lost. The DMX module uses internal buffers so that while a new DMX frame is being assembled (via the page data exchange) the module is repeatedly transmitting the last valid complete frame. A maximum of 512 channels can be transmitted to the DMX module, allowing a maximum of 5 pages of data to be sent. A cycle count is increment upon successful reception of a full frame of data from the OCS by the master module.

# 3.0. OCS - DMX exchange mechanism

The following specification shows how data is exchanged between the OCS and the DMX Master module, note that the registers referred to are with respect to the starting register in the DMX module, the actual register number will depend upon where the DMX module is mapped in the OCS register space :

***Page Code register (%AQ63) :***

The Page Code register is %AQ63 is divided into two bytes, the lower byte is the page number for which the channel data in %AQ1 to %AQ62 is valid (1-5) and the upper byte is used to as part of the handshaking to ensure that the exchange is valid. The OCS must 'toggle' the most significant bit (MSB) of this byte to validate the new data. The master module will only read the data when the Page Code register contains the page number requested in %AI1 and the toggle bit has changed since the last page read.
The Page Code register requires a special value at startup to start the master module. Once the channel count has been entered in the Channel Count Register the Page Code register must be set to 256 (100H). This forces the master module to read the channel count value and set-up the exchange for the correct number of channels.
A brief example of the correct transmission of 512 bytes is seen below.

***Channel Count Register (%AQ64):***

The Channel Count Register is %AQ64 and is set by the OCS to signal to the DMX200 how many channels of data will be sent. The Channel Count register must be set before any transmissions will occur, once set the value should not be changed, if changed the DMX200 will ignore the new value until the module is reset.
Range : 1 to 512.

***Channel Registers (%AQ1-62):***
These registers contain the channel data and are read by the master once the toggle bit and page number in the Page Code register are correct. Once the number of channels defined in the Channel Count regsister have been read the module starts to transmitt DMX frames. The channel data is packed two channels to a word with the lower byte being the lower channel ie. AQ1 contains channel 0 and channel 1 with channel 0 placed as the lower byte.

Module Status :
The master module will indicate the status of the exchange by setting following OCS registers :

***Page Code register (%AI1)***
This register will contain the page number that the master module expects channel data for. As with the the %AQ63 Page code register the lower byte contains the page number and the upper byte a toggle bit in the MSB. The toggle bit will change upon upon successful recption of new data from the OCS.

***Packet Count register (%AI2)***
This register will contain the total number of DMX packets successfully exchanged with the master module. It will roll over to 0 at 65535. The count increments when the last page of channel data has been sent to the master. It does not reflect the number of DMX packet transmissions on the bus, this will be much higher number.

Below is an example of a set of %AQ commands for a successful transmission:

1. Set the required number of channels per packet in %AQ64
2. Enter 100 in %AQ63.
3. Wait for %AI1 to update.
4. Fill %AQ1-62 with the channel data for the page indicated by %AI1.
5. Set the page number and toggle the MSB in %AQ63.
6. Repeat steps 3-5

Note : To minimise the update time for the DMX module only configure the registers that are required that is :

| Register | Size |
|---|---|
| AI | 2 |
| AQ | 64 |

Required register set.

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# 4.0. OCS-DMX Wiring details

The following connections are required to connect the DMX200 module to a DMX network :

| Type | 9-Pin D-Type Female |
|---|---|
| Signal | Pin No. |
| Screen | 5 |
| Signal- | 2 |
| Signal+ | 7 |

DMX200 Connection details.

The cable should be connected to Port 2 of the DMX200 Module.