Lighting Control Interface

HE800DMX100

This specification covers the Lighting Control Interface (DMX100) between the DMX512 receiver module and the OCS family of PLCs.

1 INTRODUCTION

The DMX512 protocol is implemented as an asynchronous embedded protocol on the ASCII 100 Smartstack module. Due to the limited register set of the ASCII modules the DMX channels are read by the OCS from the ASCII in blocks of up to one hundred and twenty channels at a time. The firmware monitors the serial port for DMX traffic and sends all valid DMX data frames to the OCS. Detected errors such as loss of traffic set all channels to zero via the firmware. The received packets counter is used to verify that data is valid; the count only increments when valid packets are detected.

2 DMX-OCS EXCHANGE MECHANISM

The following specification shows how data is exchanged between the OCS and the DMX smartstack module, note that the registers referred to are with respect to the starting register in the DMX module, the actual register number will depend upon where the DMX module is mapped in the OCS register space:

a. Command register (%AQ1

The command register is %AQ1 and it is set by the OCS to instruct the DMX module what mode to run in. The following commands are supported:

1 – Read the set of channels defined by the start address in AQ2
4 – Print all 512 channels in ASCII readable format out serial port 0 (9600 baud).

b. Start channel register (%AQ2)

This register is set by the OCS to define the block of up to 120 channels to read from the DMX module. The OCS – DMX interface is a maximum of 64 words in and out. The start channel register is %AQ2; it defines the channel number for the start of the next block (of up to 120) bytes to read from the DMX module.

Note: The first channel returned in the block is the start channel + one (e.g., Start = 0 returns channel 1, Start = 120 returns channel 121).

PRELIMINARY

c. Module Status
The DMX indicates the status of the exchange using the following registers:

Finished register (%AI61)

This register contains a copy of the last command completed. When a block of channels has been successfully sent the register is updated; it retains the previous value during execution of the command.

Start Channel register (%AI62)

This register contains a copy of the start channel number of the command just completed; it retains the previous value during execution of the command.

Number of channels register (%AI63)

This register contains the number of valid channels in the last successfully executed command. This is a maximum of 120.

Total packets received (%AI64)

This register contains the total number of DMX packets successfully received from the bus; it rolls over to 0 at 65535. The total packets received count can be used to indicate whether the data is valid. The count must increment from the last scan update or the data is invalid.

Channel registers (%AI1-%AI60)

These registers need to be read once it has been verified that the count has increased from the last scan.

Note: Beware of roll-over at 65535.

The data is packed two channels to a word with the upper byte being the lower channel (e.g., AI1 contains channel 0 and channel 1 with channel placed as the lower byte).

Note: To minimize the update time for the DMX module only configure the registers that are required as shown in Table 1.

Table 1 - Required Register Set	
Register	**Size**
AI	64
AQ	2

3 DMX-OCS WIRING DETAILS

The following connections are required to connect the DMX100 module to a DMX network.

Table 2 – DMX100 Connection Details	
Type	**9-Pin D-Type Female**
Signal	Pin No.
Screen	5
Signal-	1
Signal+	6

The cable should be connected to Port 2 of the DMX100 Module.

4 TECHNICAL SUPPORT

For assistance, contact Technical Support at the following locations:

North America:

(317) 916-4274
www.heapg.com

Europe:

(+) 353-21-4321-266
www.horner-apg.com

NOTES