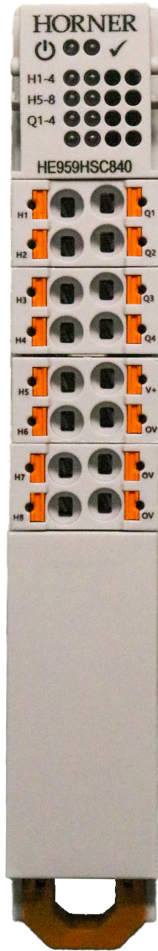




HSC840 Datasheet

MAN1423_03_EN_959HSC840_DS



compatible with **OCS I/O**

HG-1376

Part Number: HE959HSC840

User Manual and Add-Ons

Find the documents via the [Documentation Search](#).

Part #	Description
HE-FBD001	Ferrite core for filtering out electrical noise

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TECHNICAL SPECIFICATIONS

General Specifications

Required Power (steady state)	<130mA @ 5V <26mA @ 24V
Required Power (inrush)	6.2A for 300 µs
Primary Power Range	10-30VDC
Digital Inputs	8
Digital Outputs	4
Port Connectors	Phoenix Contact 2201780
Port Wiring - Digital I/O	16-24 AWG/0.2-1.5mm ²
Relative Humidity	5 to 95% non-condensing
Operating Air Temperature	-40°C (-40°F) to 60°C (140°F)
Storage Air Temperature	-40°C (-40°F) to 85°C (185°F)
Weight	88g (3.10 oz.)
Dimensions	76.5mm x 124.5mm x 19mm 3" x 4.9" x 0.75"
Mounting	35 mm DIN Rail
Housing Material	Plastic

Testing

Shock	IEC 60068-2-27
Vibration	IEC 60068-2-6
UL Environmental Ratings	Type 1, 4, 4X, 12, 12k & 13 (for indoor use only)
Certifications (UL/CE)	North America Europe

DIGITAL I/O SPECIFICATIONS

Digital DC Inputs

Inputs per Module	8	
Commons per Module	1	
Input Voltage Range	0 - 24VDC	
Absolute Maximum Voltage	32VDC	
Input Impedance	110kΩ	
Input Current	Positive Logic	Negative Logic
Minimum ON Current	0.8mA	-1.6mA
Maximum OFF Current	0.3mA	-2.1mA
Minimum ON Input (Positive Polarity) / Maximum ON Input (Negative Polarity) Parenthesis indicate the nominal input voltage.	16VDC (24V) 8VDC (12V) 3VDC (5V) 0.1VDC (Zero Crossing)	8VDC (24V) 4VDC (12V) 0.8VDC (5V) -0.1VDC (Zero Crossing)
Maximum OFF Input (Positive Polarity) / Minimum OFF Input (Negative Polarity) Parenthesis indicate the nominal input voltage.	8VDC (24V) 4VDC (12V) 0.8VDC (5V) -0.1VDC (Zero Crossing)	16VDC (24V) 8VDC (12V) 3VDC (5V) 0.1VDC (Zero Crossing)
Input Filter	500kHz 50kHz 5kHz	
OFF to ON Response	2ns minimum	
ON to OFF Response	2ns minimum	
HSC Maximum Frequency	500kHz	
Galvanic Isolation	None	
Logic Polarity	Selectable (Common to all eight inputs)	
I/O Indication	Status LED per Input	
High Speed Counter (HSC)	8	

Digital DC Outputs

Outputs per Module	4
Commons per Module	1
Output Type	Sourcing
Absolute Maximum Voltage	28VDC
Output Protection	Short Circuit
Maximum Output Current/Point	0.5A
Maximum Total Current	2A Total Current
Maximum Output Supply	30VDC
Minimum Output Supply	10VDC
Maximum Voltage Drop at Rated Current	0.25VDC
Minimum Load	None
I/O Indication	Status LED per output
Galvanic Isolation	None
OFF to ON Time (typical)	500ns min
ON to OFF Time (typical)	500ns min
Minimum PWM Pulse Width	1 μ s
Maximum PWM Frequency	500 kHz
Output Characteristics	Current Sourcing (Positive Logic)

WIRING AND LED INDICATORS

Digital Inputs & Outputs

Digital Inputs		Digital Outputs																																					
8 INPUTS		4 Outputs																																					
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left;">SIGNAL</th> <th style="text-align: left;">DESCRIPTION</th> </tr> </thead> <tbody> <tr><td>H1</td><td>Input 1</td></tr> <tr><td>H2</td><td>Input 2</td></tr> <tr><td>H3</td><td>Input 3</td></tr> <tr><td>H4</td><td>Input 4</td></tr> <tr><td>H5</td><td>Input 5</td></tr> <tr><td>H6</td><td>Input 6</td></tr> <tr><td>H7</td><td>Input 7</td></tr> <tr><td>H8</td><td>Input 8</td></tr> </tbody> </table>	SIGNAL	DESCRIPTION	H1	Input 1	H2	Input 2	H3	Input 3	H4	Input 4	H5	Input 5	H6	Input 6	H7	Input 7	H8	Input 8	<p style="text-align: center; font-size: small;">HG-1367</p>	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left;">SIGNAL</th> <th style="text-align: left;">DESCRIPTION</th> </tr> </thead> <tbody> <tr><td>Q1</td><td>Output 1</td></tr> <tr><td>Q2</td><td>Output 2</td></tr> <tr><td>Q3</td><td>Output 3</td></tr> <tr><td>Q4</td><td>Output 4</td></tr> <tr><td>V+</td><td>V+ Input for Outputs 1-4</td></tr> <tr><td>OV</td><td>Common</td></tr> <tr><td>OV</td><td>Common</td></tr> <tr><td>OV</td><td>Common</td></tr> </tbody> </table>	SIGNAL	DESCRIPTION	Q1	Output 1	Q2	Output 2	Q3	Output 3	Q4	Output 4	V+	V+ Input for Outputs 1-4	OV	Common	OV	Common	OV	Common	<p style="text-align: center; font-size: small;">HG-1368</p>
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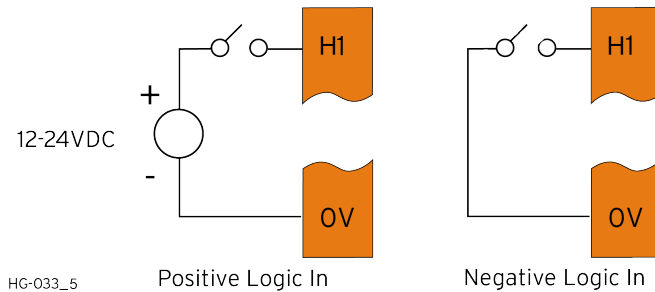


Use 75°C copper conductors only.

Positive & Negative Logic

The setting in the Cscape Hardware Configuration for the Digital Inputs must match the wiring used in order for the correct input states to be registered. The state of the inputs is in registers %H1 – %H8.

Digital inputs may be wired in either Positive Logic or Negative Logic.



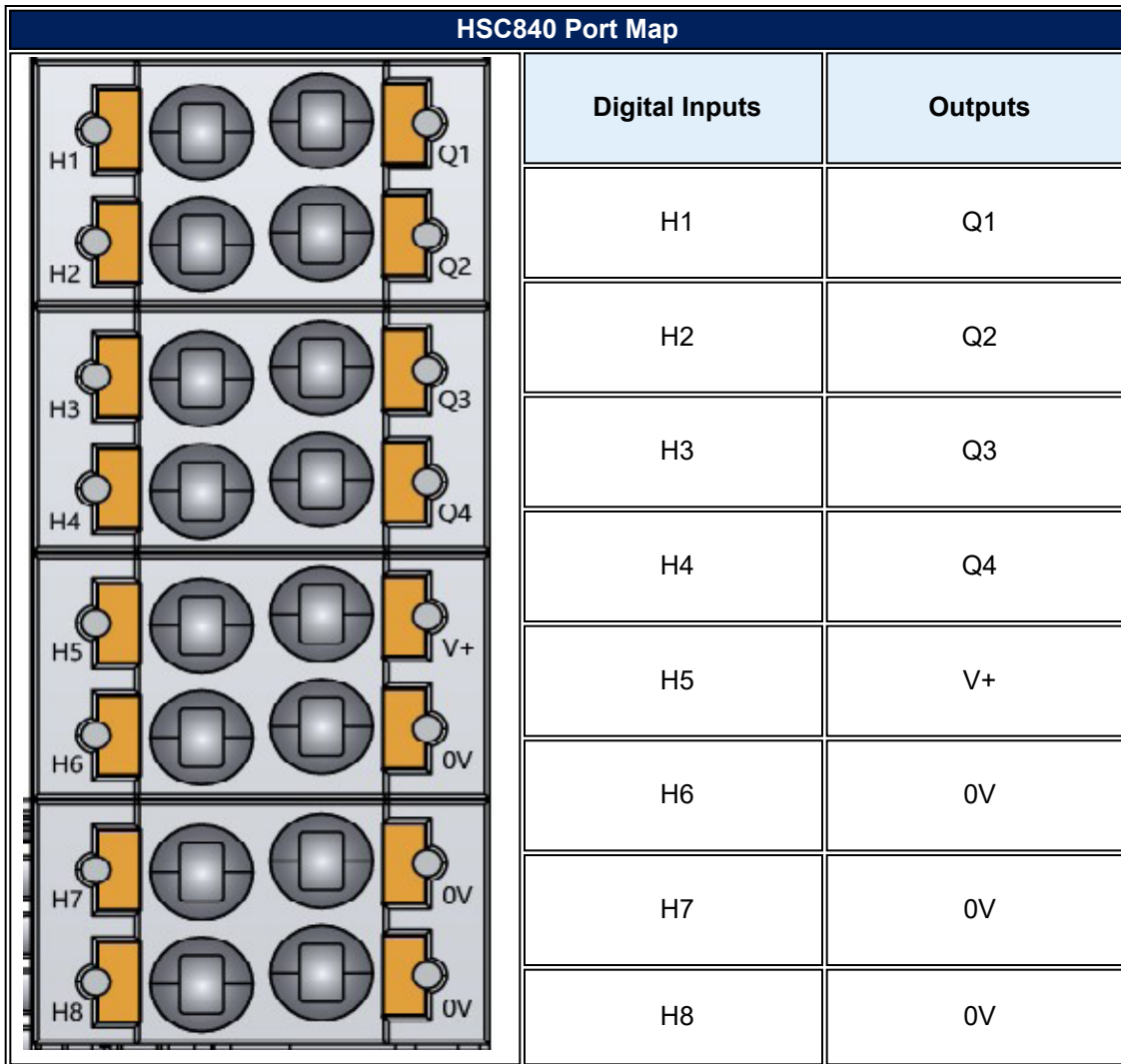
Diagnostic LED Indicators

Status	OK LED
OFF	Power Up
ON	I/O Module Running Normally
BLINK (1Hz)	One of the following errors: <ol style="list-style-type: none"> a. Communication between IO Base and IO Module (IO ERROR) b. No Configuration c. OCS idle mode

Built-In I/O Connectors

Digital I/O Functions

Description	
H1-H8	Digital Inputs
Q1-Q4	Digital Outputs
V+	External Power
0V	Common



HIGH SPEED COUNTER PROGRAMMING & OPERATION

Overview

The OCS I/O HSC840 module supports High Speed Counting (HSC) I/O functions and Pulse Width Modulation (PWM) Output functions. The HSC functions include internal timing, frequency, totalizing, pulse width/period, and quadrature measurement. The PWM functions include traditional PWM outputs with variable period and duty cycle. This chapter describes the operation of these high-level I/O functions.

Glossary

Term	Definition
Accumulator	Register used to accumulate or store up a sum or count of many items or events.
Clean	A special function to zero the value in a specific register. (Not used with Frequency or Period Measurement.)
Disable	A special function to prevent the counter from running.
Encoder	A sensor or transducer for converting rotary motion or position to a series of electronic pulses.
Frequency Input	The number of times an electromagnetic signal repeats an identical cycle in a unit of time, usually one second.
Latch (Strobe)	A special function that uses a digital logic circuit to store one or more bits. A latch has a data input, a clock input and an output. When the clock input is active, data on the input is "latched" or stored and transferred to the output register either immediately or when the clock input goes inactive. The output retains its value until the clock goes active again.
Marker	Input into the OCS that indicates a particular position. Typically, an encoder has a marker output that represents a specific point in the rotation.
Polarity	A polarity dropdown menu box is associated with each function and indicates the manner in which the trigger happens (e.g., High level, Low Level, Falling Edge, Rising Edge).
Preload (Load)	A special function used to trigger loading of a value into a register upon an event. (Not used with Frequency or Period Measurement.)
Quadrature	A high-speed device that expresses the phase relationship between two periodic quantities of the same period when the phase difference between them is one fourth of a period. A coupler in which the two output signals are 90° out of phase.
Totalizer	A counter that sums the total number of cycles applied to its input.

Functions

The HSC840 supports eight very high speed, configurable counters. Each of the eight counters can run in one of five modes. Those modes are Totalizer, Frequency Counter, Pulse Width Measurement, Period Measurement, and Quadrature measurement. For some modes, more than one HSC input may be consumed. The measurement values are provided to ladder in a %AI register.

Frequency Measurements

In frequency mode, the frequency of the input signal is written to the accumulator in terms of hertz (cycles/second). When using frequency mode, four update selections are provided that specify the width of the sample window. NOTE: Selecting a shorter sample window provides a quicker measurement (faster response) but lowers the frequency accuracy (resolution) and increases the minimum frequency measurement limit.

Totalize Mode

In totalize mode, the accumulator is incremented or decremented each time the input transitions in a specific direction, the Counters trigger on the rising edge of the signal.

The totalizer supports the following modes:

Term	Definition
Internal	This mode maps the input to the counter to an internal 10MHz or 1MHz clock. The special functions can be used to accurately time events.
Count Up	This increments the accumulator when the input is enabled. Up to two inputs can be assigned. Either input can cause the counter to increment. The second input can be disabled through the logic.
Count Down	This decrements the accumulator when the input is enabled. Up to two inputs can be assigned. Either input can cause the counter to decrement. The second input can be disabled through the logic.
Up/Down (Input 1 UP/Input 2 Down)	In this mode, Input 1 (assigned to any input) increments the counter, while Input 2 (assigned to any input) decrements the counter.
Clk/Dir (Input 1 Clk, Input 2 Dir)	This mode uses input 1 as a clock signal to increment or decrement the counter and then uses input 2 to determine the direction. Input 2 disabled increments the counter, while input 2 enabled decrements the counter.

Table 1.0. Totalize functions

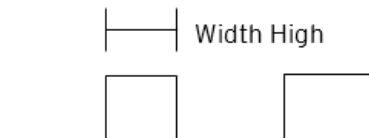
NOTE: See Table 1.0. for the special features enabled in Totalize mode.

The totalize function also supports an option which compares the current accumulator value with a supplied Preset Value (PV) that is provided through a %AQ, and drives a physical digital output based on the Counter reaching or exceeding the PV value. To enable this function, the corresponding PWM function output (Q1 to Q4) must be configured for HSCx Output. Preset values may be modified during run-time. A preset value of zero resets the totalizer compare function and sets the output low.

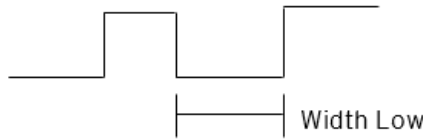
Pulse Width Measurement (PWM)

In pulse width measurement mode, the high-speed input can measure the width of a pulse stream in one of two modes and provides a continuous indication of the last sampled value: "Glossary" on the previous page

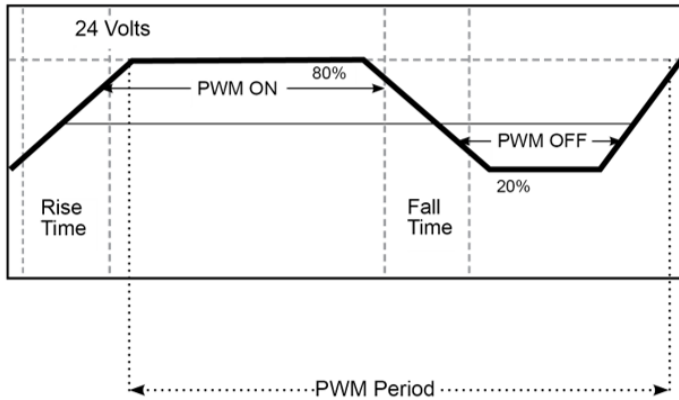
Width High 1 μ s Counts – In this sub-mode the accumulator value will contain the number of 1 μ s counts the pulse is high.



Width Low 1 μ s Counts - In this sub-mode the accumulator value will contain the number of 1 μ s counts the pulse is low.



PWM Output Waveform

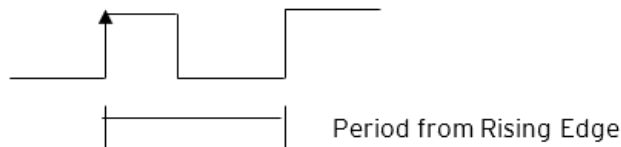


PWM Output Waveform Table	
Rise Time	150ns Max
Fall Time	150ns Max
PWM Period	Frequency = $\frac{1}{Period}$

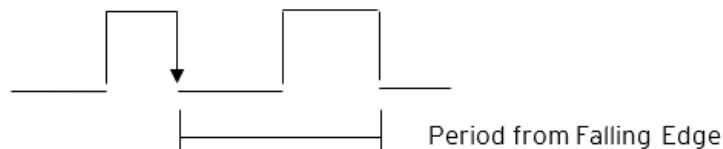
Period Measurement

In period measurement mode, the high-speed input can measure the period of a pulse stream in one of two modes and provides a continuous indication of the last sampled value: "Glossary" on page 7

Period Rising Edges 1 μ s Counts – In this sub-mode the period of the input signal is reported in one (1) μ s units. The period measurement will start on the rising edge of the input.

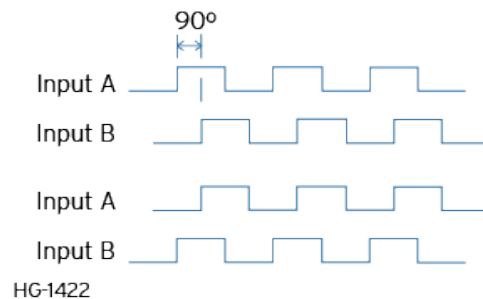


Period Falling Edges 1 μ s Counts – In this sub-mode the period of the input signal is reported in one (1) μ s units. The period measurement will start on the falling edge of the input.



Quadrature Mode

Quadrature mode uses two HSC inputs, any of the eight HSC inputs can be assigned for this purpose. The accumulator will automatically increment or decrement based on the rotation phase of the two inputs. See the following example for more details. Two modes are available for quadrature that select whether the accumulator counts up or down when the phase of Input 1 leads Input 2. Confirm with the encoder documentation to determine the output form it uses. Using the above waveforms and a HSC input configuration of “Quadrature” - “1 leads 2, count up,” the accumulator will count up when 1 is rising and 2 is low, 1 is high and 2 is rising, 1 is falling and 2 is high, and when 1 is low and 2 is falling. This results in 4 counts per revolution. So in order to determine the number of cycles, the accumulator must be divided by 4. Marker reset operation is configured in the special operations and can be assigned to any of the eight high speed inputs or can be assigned to be controlled by a “Q” bit in ladder.



Register Match

Totalizer & Quadrature counter modes support a register match function with the following features.

- When the accumulator value matches either the Match 1 or Match 2 value configured in the corresponding %AQ registers, a high-speed output can Turn On, Turn Off, or Toggle.
- An internal %I register mirrors the output state whether the high-speed output is configured or not. The output can be reset in program logic using the corresponding %Q registers. The outputs operate as high-speed outputs, independent of the controller scan rate, when configured as ‘HSC Output’ in the Digital Out/PWM configuration in Cscape.
- The High-Speed Output state is reflected in the status register “High Speed Out”, e.g. %I0009 %I1603 for Counter 1 (the update speed of the status bit is scan rate dependent).
- The High-Speed Output can be reset through ladder with the assigned output, e.g. %Q0022% Q1606 for Counter 1
- Both Match 1 and Match 2 values will trigger the match function.
- If the output is already triggered by any Match register while using ‘Turn On’ or ‘Turn Off’ modes, subsequent matches will not affect the output.
- If using ‘Toggle’ mode, every match of either Match value will toggle the output to the opposite state.

HSC Functions

The high-speed input on the OCS supports many optional tasks. All of which can be disabled, or set to an internal pre-assigned register (Assigned %Q) or to one of the external high speed inputs (External Input #1 - 8), or they can be set as an “overflow” or “underflow” interrupt meaning that they will occur when either the Overflow or Underflow input has been activated.

- **Disable:** When the Disable function is active, it will “disable” the high-speed inputs and no longer count pulses until it is re-enabled.
- **Latch:** When the Latch function is active, it takes the current value of the Accumulator and copies it into the “Latch Value” register.
- **Preload:** When the preload function is active, it will take the value from the “Preload” register and put it into the “Accumulator” for the corresponding Counter.
- **Clear:** When the clear function is active, it will move a value of 0 into the “Accumulator” for the corresponding counter.
- **Marker:** When the marker function is enabled, it acts as a dynamic enable/disable for the Disable, Latch, Preload, and Clear functions. If the marker is enabled and an “Assigned %Q” is selected, then both the “Disable” and the “Disable Marker” bits need to be set high in order to disable the high-speed input. If the Marker is set for one of the inputs, then the input will need to be “High” in order to use any of the Disable, Clear, Preload, or Latch functions.

Mode	Clear	PreLoad	Latch	Disable	Match	Marker
Frequency	-	-	Yes	Yes	-	-
Totalizer	Yes	Yes	Yes	Yes	Yes	
Pulse Width	-	-	Yes	Yes	-	-
Period	-	-	Yes	Yes	-	-
Quadrature	Yes	Yes	Yes	Yes	Yes	Yes

Table 2.0 Features supported by the HSC modes

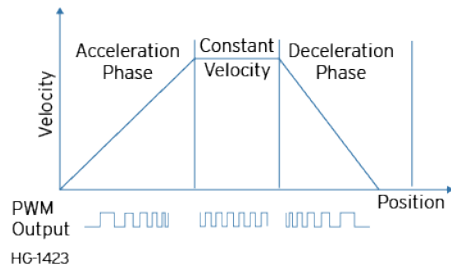
High Speed Output Functions On units that support high-speed output functions, four dedicated outputs are available that can be configured for one of five modes of operation. Those modes are Normal, PWM, HSC Match, Stepper and PTO:

- **- Normal** When any of Q1 to Q4 are configured for Normal operation, the corresponding logic digital output registers %Q1 to %Q4 drives the respective output.
- **- PWM** When any of Q1 to Q4 are configured for PWM, the PWM function drives that respective output. Any of the four PWM channels may be individually enabled and can have independent frequency and duty cycles. The PWMs require two parameters (%AQs) to be set for operation. These parameters may be set at run-time. Duty Cycle – The Duty Cycle is a 32-bit value from 0 to 32,000 indicating the relative duty cycle of the output. For example, a value of 8000 would indicate a 25% duty cycle, a value of 16,000 would indicate a 50% duty cycle. Zero (0) turns the output off, 32,000 turns the output on.
- **- High Speed Counter Match** when any of Q1 to Q4 are configured for HSC Output operation, their output state is based on a comparison between the counter accumulator and match registers.
- **- Stepper Function** the OCS supports four stepper functions, one on each high-speed output. The Stepper requires five parameters (%AQs) to be set for operation. These parameters may be set at run-time but are 'latched' when the stepper is commanded to start: Start Frequency (pulses per second) sets the frequency for the first cycle during the acceleration phase and the frequency of the last cycle during the deceleration phase. When an acceleration or deceleration count is specified, the Start Frequency must be greater than 0 and must not exceed the run frequency or an error is generated. Run Frequency (pulses per second) sets the frequency for the last cycle during the acceleration phase, the consistent frequency during the run phase, and the frequency of the first cycle during the deceleration mode. The Run Frequency must be greater than 0 and must not exceed 5000Hz (standard). Acceleration Count sets the number of cycles to occur within the acceleration phase. The frequency of the cycles within this mode will vary linearly between the specified Start

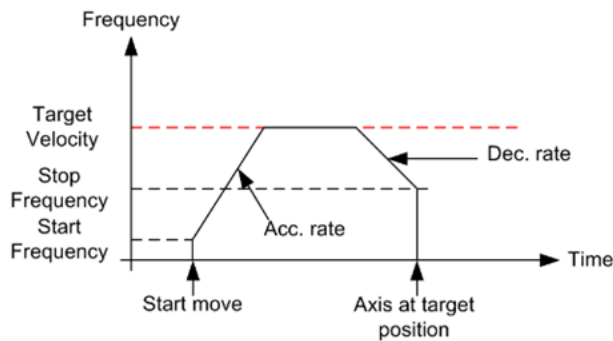
and Run frequency. The Accel count must not equal 1 or an error is generated. Setting this value to zero disables this phase. Run Count sets the number of cycles to occur within the run phase. The frequency of the cycles within this mode is constant at the specified Run frequency. The Run count may be any value. Setting this value to zero disables this phase. Deceleration Count Sets the number of cycles to occur within the deceleration phase. The frequency of the cycles within this phase will vary linearly between the specified Run and Stop frequency. The Decel count must not equal 1 or an error is generated. Setting this value to zero disables this phase. The stepper provides two Boolean registers to provide stepper status: Ready/Done - a high indication on this register indicates the stepper sequence can be started (i.e. not currently busy) and also when the move is completed. Error - a high indication on this register indicates that one of the analog parameters specified above is invalid or the stepper action was aborted before the operation was complete. This register is cleared on the next start command if the error was corrected. The stepper requires one discrete register to control the stepper action. Setting this register starts the stepper cycle. This register must remain set to complete the entire cycle. Clearing this register before the cycle is complete aborts the step sequence and sets the error bit.

NOTE: Setting the PLC mode to stop while the stepper is in operation causes the stepper output to immediately drop to zero and the current stepper count to be lost.

NOTE: The stepper output level may cause damage or be incompatible with some motor drive inputs. Consult drive documentation to determine if output level and type is compatible.



- PTO Function. This function is similar to the Stepper but uses different parameters to generate the output profile. The profile is as follows:



- Frequency (run frequency)
- Number of Pulses
- Acceleration Time(ms)
- Deceleration Time(ms)
- Direction – Forward/Reverse
- Duty cycle is fixed at 50%



When PTO output is triggered, it attains the frequency defined in the Acceleration time set by the user and continues to generate pulses at the set frequency and slows down to a stop in the Deceleration time defined by the user.

HSC Functions Register Map

Register assignments for the high speed I/O are made in the Cscape Hardware Config, CAN1 (CsCAN) I/O tab, OCSIO tab. The starting address offsets are configured specifically in the HE959CNX1xx CsCAN base module.

Register	Description
%Alx+0-1	HSC1 Accumulator
%Alx+2-3	HSC1 Latched Accumulator
%Alx+4-5	HSC2 Accumulator
%Alx+6-7	HSC2 Latched Accumulator
%Alx+8-9	HSC3 Accumulator
%Alx+10-11	HSC3 Latched Accumulator
%Alx+12-13	HSC4 Accumulator
%Alx+14-15	HSC4 Latched Accumulator
%Alx+16-17	HSC5 Accumulator
%Alx+18-19	HSC5 Latched Accumulator
%Alx+20-21	HSC6 Accumulator
%Alx+22-23	HSC6 Latched Accumulator
%Alx+24-25	HSC7 Accumulator
%Alx+26-27	HSC7 Latched Accumulator
%Alx+28-29	HSC8 Accumulator
%Alx+30-31	HSC8 Latched Accumulator

Register	Description
%AQx+0-1	HSC1 Preload Value
%AQx+2-3	HSC1 Match 1 Value
%AQx+4-5	HSC1 Match 2 Value
%AQx+6-7	HSC2 Preload Value
%AQx+8-9	HSC2 Match 1 Value
%AQx+10-11	HSC2 Match 2 Value
%AQx+12-13	HSC3 Preload Value
%AQx+14-15	HSC3 Match 1 Value
%AQx+16-17	HSC3 Match 2 Value
%AQx+18-19	HSC4 Preload Value
%AQx+20-21	HSC4 Match 1 Value
%AQx+22-23	HSC4 Match 2 Value
%AQx+24-25	HSC5 Preload Value
%AQx+26-27	HSC5 Match 1 Value
%AQx+28-29	HSC5 Match 2 Value

%AQx+30-31	HSC6 Preload Value
%AQx+32-33	HSC6 Match 1 Value
%AQx+34-35	HSC6 Match 2 Value
%AQx+36-37	HSC7 Preload Value
%AQx+38-39	HSC7 Match 1 Value
%AQx+40-41	HSC7 Match 2 Value
%AQx+42-43	HSC8 Preload Value
%AQx+44-45	HSC8 Match 1 Value
%AQx+46-47	HSC8 Match 2 Value

Register	Description
HSC1	
%Qx+0	HSC1 Latch Trigger
%Qx+1	HSC1 Preload Trigger
%Qx+2	HSC1 Clear Trigger
%Qx+3	HSC1 Disable Counter
%Qx+4	HSC1 Direction
%Qx+5	HSC1 Underflow/Overflow/HSCQ Reset (1-Reset)
%Qx+6	HSC1 Preload Disable (1-Disable)
%Qx+7	HSC1 Latch Disable (1-Disable)
HSC2	
%Qx+16	HSC2 Latch Trigger
%Qx+17	HSC2 Preload Trigger
%Qx+18	HSC2 Clear Trigger
%Qx+19	HSC2 Disable Counter
%Qx+20	HSC2 Direction
%Qx+21	HSC2 Underflow/Overflow/HSCQ Reset (1-Reset)
%Qx+22	HSC2 Preload Disable (1-Disable)
%Qx+23	HSC2 Latch Disable (1-Disable)
HSC3	
%Qx+32	HSC3 Latch Trigger
%Qx+33	HSC3 Preload Trigger
%Qx+34	HSC3 Clear Trigger
%Qx+35	HSC3 Disable Counter
%Qx+36	HSC3 Direction
%Qx+37	HSC3 Underflow/overflow/HSCQ Reset (1-Reset)
%Qx+38	HSC3 Preload Disable (1-Disable)
%Qx+39	HSC3 Latch Disable (1-Disable)

HSC4	
%Qx+48	HSC4 Latch Trigger
%Qx+49	HSC4 Preload Trigger
%Qx+50	HSC4 Clear Trigger
%Qx+51	HSC4 Disable Counter
%Qx+52	HSC4 Direction
%Qx+53	HSC4 Underflow/Overflow/HSCQ Reset (1-Reset)
%Qx+54	HSC4 Preload Disable (1-Disable)
%Qx+55	HSC4 Latch Disable (1-Disable)
HSC5	
%Qx+64	HSC5 Latch Trigger
%Qx+65	HSC5 Preload Trigger
%Qx+66	HSC5 Clear Trigger
%Qx+67	HSC5 Disable Counter
%Qx+68	HSC5 Direction
%Qx+69	HSC5 Underflow/Overflow/HSCQ Reset (1-Reset)
%Qx+70	HSC5 Preload Disable (1-Disable)
%Qx+71	HSC5 Latch Disable (1-Disable)
HSC6	
%Qx+80	HSC6 Latch Trigger
%Qx+81	HSC6 Preload Trigger
%Qx+82	HSC6 Clear Trigger
%Qx+83	HSC6 Disable Counter
%Qx+84	HSC6 Direction
%Qx+85	HSC6 Underflow/Overflow/HSCQ Reset (1-Reset)
%Qx+86	HSC6 Preload Disable (1-Disable)
%Qx+87	HSC6 Latch Disable (1-Disable)
HSC7	
%Qx+96	HSC7 Latch Trigger
%Qx+97	HSC7 Preload Trigger
%Qx+98	HSC7 Clear Trigger
%Qx+99	HSC7 Disable Counter
%Qx+100	HSC7 Direction
%Qx+101	HSC7 Underflow/Overflow/HSCQ Reset (1-Reset)
%Qx+102	HSC7 Preload Disable (1-Disable)
%Qx+103	HSC7 Latch Disable (1-Disable)
HSC8	
%Qx+112	HSC8 Latch Trigger
%Qx+113	HSC8 Preload Trigger

%Qx+114	HSC8 Clear Trigger
%Qx+115	HSC8 Disable Counter
%Qx+116	HSC8 Direction
%Qx+117	HSC8 Underflow/Overflow/HSCQ Reset (1-Reset)
%Qx+118	HSC8 Preload Disable (1-Disable)
%Qx+119	HSC8 Latch Disable (1-Disable)

Register	Description
HSC1	
%lx+0	HSC1 Overflow Flag
%lx+1	HSC1 Underflow Flag
%lx+2	HSC1 HSCQ
%lx+3	HSC1 Reserved
HSC2	
%lx+4	HSC2 Overflow Flag
%lx+5	HSC2 Underflow Flag
%lx+6	HSC2 HSCQ
%lx+7	HSC2 Reserved
HSC3	
%lx+8	HSC3 Overflow Flag
%lx+9	HSC3 Underflow Flag
%lx+10	HSC3 HSCQ
%lx+11	HSC3 Reserved
HSC4	
%lx+12	HSC4 Overflow Flag
%lx+13	HSC4 Underflow Flag
%lx+14	HSC4 HSCQ
%lx+15	HSC4 Reserved
HSC5	
%lx+16	HSC5 Overflow Flag
%lx+17	HSC5 Underflow Flag
%lx+18	HSC5 HSCQ
%lx+19	HSC5 Reserved
HSC6	
%lx+20	HSC6 Overflow Flag
%lx+21	HSC6 Underflow Flag
%lx+22	HSC6 HSCQ
%lx+23	HSC6 Reserved

HSC7	
%Ix+24	HSC7 Overflow Flag
%Ix+25	HSC7 Underflow Flag
%Ix+26	HSC7 HSCQ
%Ix+27	HSC7 Reserved
HSC8	
%Ix+28	HSC8 Overflow Flag
%Ix+29	HSC8 Underflow Flag
%Ix+30	HSC8 HSCQ
%Ix+31	HSC8 Reserved

High Speed Output Functions

All outputs can be configured for one of three modes of operation. Those modes are Normal, PWM and HSC Match.

Normal

When either Q1 to Q4 is configured for Normal operation, the digital output registers %Q1 to %Q4 drives that respective output.

PWM

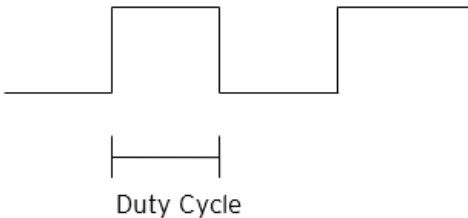
When either Q1 to Q4 is configured for PWM, the PWM function drives that respective output. All PWM channels may be individually enabled and can have independent frequency and duty cycles.

The PWMs require two parameters (%AQs) to be set for operation. These parameters may be set at run-time.

Duty Cycle

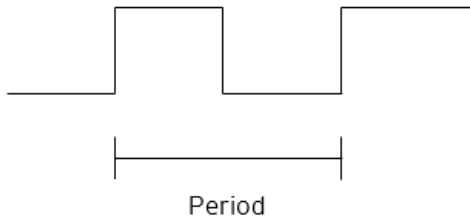
The Duty Cycle is a 32-bit value from 0 to 32,000 indicating the relative duty cycle of the output. For example, a value of 8000 would indicate a 25% duty cycle, and a value of 16,000 would indicate a 50% duty cycle.

The value 0 turns the output off, and 32,000 turns the output on.



Frequency

The Frequency is a 32-bit value indicating the output frequency in Hertz. One over the frequency is the period.



At controller power-up or during a download, the PWM output is maintained at zero until both the Frequency and the Duty cycle are loaded with non-zero values. When the controller is placed in stop mode, the state of the PWM outputs is dependent on the PWM State on Controller Stop configuration. This configuration allows for either hold-last-state or specific frequency and duty cycle counts. Specifying zero for either the period or duty causes the PWM output to remain low during stop mode.

High Speed Counter Match

When either Q1 to Q4 is configured for HSC Output operation, their output state is based on a comparison between the counter accumulator and match registers. See details above in the high-speed input section.

High Speed Output Functions Register Map

The register assignments for the high speed I/O can be moved via a setting in Cscape. The values shown are the **default** values and may not match the same starting point as the values shown below.

PWM I/O Register Map	
Register	Description
%AQx+48-49	PWM1 Duty Cycle
%AQx+50-51	PWM1 Frequency
%AQx+52-53	PWM2 Duty Cycle
%AQx+54-55	PWM2 Frequency
%AQx+56-57	PWM3 Duty Cycle
%AQx+58-59	PWM3 Frequency
%AQx+60-61	PWM4 Duty Cycle
%AQx+62-63	PWM4 Frequency

PWM Examples

Example 1	Duty Cycle	Frequency
To get a 50% Duty Cycle @ 10kHz waveform on PWM1	Set %AQ151-152 = 16,000	Set %AQ153-154 = 10,000

Example 2	Duty Cycle	Frequency
To turn PWM 1 output ON all the time	Set %AQ151-152 = 32,000	Set %AQ153-154 = Any Value

Example 3	Duty Cycle	Frequency
To turn PWM 1 output OFF all the time	Set %AQ151-152 = 0	Set %AQ153-154 = Any Value

SAFETY & MAINTENANCE

Warnings

1. To avoid the risk of electric shock or burns, always connect the safety (or earth) ground before making any other connections.
2. To reduce the risk of fire, electrical shock, or physical injury, it is strongly recommended to fuse the voltage measurement inputs. Be sure to locate fuses as close to the source as possible.
3. Replace fuse with the same type and rating to provide protection against risk of fire and shock hazards.
4. In the event of repeated failure, do **NOT** replace the fuse again as repeated failure indicates a defective condition that will **NOT** clear by replacing the fuse.
5. Only qualified electrical personnel familiar with the construction and operation of this equipment and the hazards involved should install, adjust, operate, or service this equipment.
6. Read and understand this manual and other applicable manuals in their entirety before proceeding. Failure to observe this precaution could result in severe bodily injury or loss of life.
7. **WARNING:** Battery may explode if mistreated. Do not recharge, disassemble, or dispose of in fire.
8. **WARNING:** EXPLOSION HAZARD - Batteries must only be changed in an area known to be non-hazardous.
9. **WARNING:** Do not disconnect while circuit is live unless area is known to be non-hazardous.

FCC Compliance

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

Precautions

All applicable codes and standards need to be followed in the installation of this product. Adhere to the following safety precautions whenever any type of connection is made to the module:

1. Connect the safety (earth) ground on the power connector first before making any other connections.
2. When connecting to the electric circuits or pulse-initiating equipment, open their related breakers.
3. Do NOT make connection to live power lines.
4. Make connections to the module first; then connect to the circuit to be monitored.
5. Route power wires in a safe manner in accordance with good practice and local codes.
6. Wear proper personal protective equipment including safety glasses and insulated gloves when making connections to power circuits.
7. Ensure hands, shoes, and floor are dry before making any connection to a power line.
8. Make sure the unit is turned OFF before making connections to terminals.
9. Make sure all circuits are de-energized before making connections.
10. Before each use, inspect all cables for breaks or cracks in the insulation. Replace immediately if defective.
11. Use copper conductors in field wiring only, 60/75°C.
12. Use caution when connecting controllers to PCs via serial or USB (if present). PCs, especially laptops, may use “floating power supplies” that are ungrounded. This could cause a damaging voltage potential between the laptop and controller. Ensure the controller and laptop are grounded for maximum protection. If USB is present, consider using a USB isolator due to voltage potential differences as a preventative measure.



Technical Support

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